Feature Differences Between 21554 and 21555 Non-Transparent PCI-to-PCI Bridges

Application Note

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1.0 Introduction

This document discusses the features that the users should consider when adapting a 21555 bridge into a design for a 21554 bridge. By installing a 21555 in place of a 21554, the design team can utilize several new features that are described in this document. Look for a “New Feature:” caption in the margins of the document or in tables for descriptions of the new features.

The 21555 is very similar in form and function to the 21554, having the same basic pinout. However, there are software changes and possibly other hardware issue that may need to be addressed.

Please refer to the *21555 Non-Transparent PCI-to-PCI Bridge Data Sheet* for more specific details regarding the 21555 bridge.

1.1 Product Marking

Figure 1 shows the marking that is printed on the top of the 21555 package.

Figure 1. Packaging Details

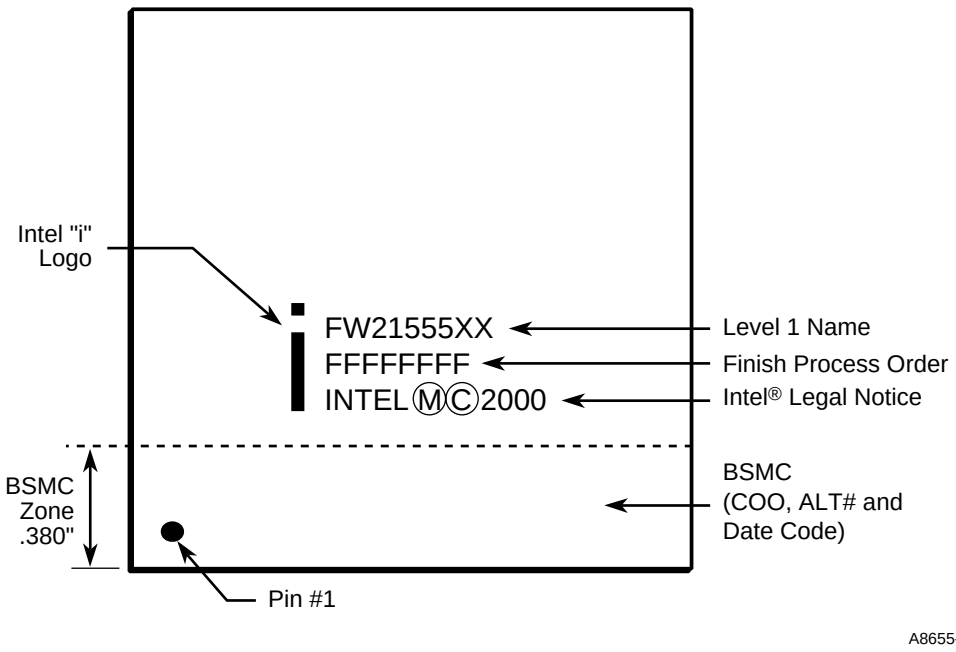


Table 1. Classification Chart

Level 1 Name	Speed	REV	Version	Level 3 Name
FW21555AA	33 MHz	A	304 PBGA	FW215551A
FW21555BA	66 MHz	A	304 PBGA	FW215551A

1.2 21555 Compatibility for Existing 21554 Designs

The 21555 bridge is very similar to the 21554 bridge in both pin out design and function but there are also significant differences between the two devices. There are two versions of the 21555 bridge: FW21555AA and FW21555BA

The following 21555 features result in a more flexible part to meet even more application needs:

- Clocking speeds for the FW21555AA version of the bridge range from 0 to 33 MHz in synchronous mode or up to a 2.5 to 1 clock ratio from primary to secondary or secondary to primary inputs in asynchronous mode up to 33MHz maximum.

  Clocking speeds for the FW21555BA version of the bridge range from 0 to 66MHz in synchronous mode or up to a 2.5 to 1 clock ratio from primary to secondary or secondary to primary inputs in asynchronous mode up to 66MHz maximum.

- The 21555 **s_rst_in_l** pin has been added and the corresponding 21554 **vdd** pin replaced. If not used, this pin should be tied high. If the 21555 is used in place of a 21554, the s_rst_in_l pin will be connected to the vdd pad and thus tied high, disabling the s_rst_in_l for backward compatibility with the 21554.

  Refer to the *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual* for specific details.

- Primary to secondary synchronous clocking divide by two (2) for 66MHz primary and 33MHz secondary operation.
- Generic memory-mappable Own Bit semaphore.
- Secondary configuration space write access (to write only from secondary registers) from the primary interface using the indirect configuration mechanism and 21555 self-decode.
- Selectable bus parking at the 21555 or at the last master.
- Improved **vio** circuits eliminate power sequencing requirements.
- Disable capability for the transaction time-out counters.
- Expanded page sizes to 32-Mbytes 64 pages for the upstream lookup (LUT) table enabling access to a total of 4Gb of memory upstream using all of the upstream bars.
- Improved hot swap support.
- The 21555 supports Cache Line Sizes (CLSs) of 8, 16, 32. CLS 4 is not supported in the 21555. Tables 16 and 17 give more information on CLS.

Important: *Customers must update the software to recognize the new Device ID and Vendor ID data.*

Notes

- See the arbitration descriptions surrounding **s_m66ena**. This signal should be tied low for 33MHz secondary PCI clock operation with external arbiter signal pairs [0:8]. When **s_m66ena** is tied high for 66MHz secondary PCI clock operation arbiter signal pairs [5:8] are disabled.
- Refer to the 21555 Data Sheet for new the latest information on AC, DC, and timing parameters, which differ from the 21554. Also included is a section about 66MHz timing for the 21555. This data is beyond the scope of this document.

- See the arbitration descriptions surrounding **s_m66ena**. This signal should be tied low for 33MHz secondary PCI clock operation with external arbiter signal pairs [0:8]. When **s_m66ena** is tied high for 66MHz secondary PCI clock operation arbiter signal pairs [5:8] are disabled.
- Refer to the 21555 Data Sheet for new the latest information on AC, DC, and timing parameters, which differ from the 21554. Also included in the data sheet is a section about 66MHz timing for the 21555. This data is beyond the scope of this document.
- The 21554 allowed 0 to 33MHz on the primary input and 0 to 33 MHz on the secondary input however both versions of the 21555 bridge require a maximum clock frequency ratio of 2.5 to 1 on secondary to primary or primary to secondary inputs in asynchronous mode. Refer to the *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual* for specific details.

1.3 New Features Technical Descriptions and Benefits

This section directs you to descriptions of new or enhanced features in the 21555:

- Section 1.3.1, "Sequencing Vdd with Respect to Vio is Not Required on the 21555".
- Section 1.3.2, "Miscellaneous Features".
- Table 3, "New JTAG Signal Requirement".
- Table 4, "Secondary Bus Feature".
- Table 5, "Bus Arbiter and Clock Output Features".
- Table 6, "ROM Interface Signal Features".

1.3.1 Sequencing Vdd with Respect to Vio is Not Required on the 21555

Table 2 describes the power sequencing between voltage on **vdd** and **vio** and discusses when to consider a 1K Ohm series resistor between **vdd** and **vio**.

Table 2. Power Sequencing Vdd with Respect to Vio on the 21554[a]

vdd	vio	Series	1.8V Separation	Description
3.3	0	No	No	When vdd is at 3.3 volt and **vio** is still at 0 volt, the PCI clamp will turn on and start clamping the output voltage. At two diode drops or about 1.5 volts. No reliability problem exists however output signals will not be a valid logic level.
3.3	3.3	No	No	With vdd and **vio** at 3.3 volts the chip will function normally except when signals have overshoots above the **vio** voltage. The clamp will turn on and the output voltage starts clamping at the **vio** level. This configuration is not recommended. Connect **vio** to 5 volt.
0	3.3	Yes	No	With vdd at 0 volts and **vio** at 3.3 volts, large current could flow from **vio** into a series of diodes inside the bridge. When an application presents these conditions a 1K series resistor will limit the current.
3	5	Yes	Yes	When the recommended 1.8 volt separation between **vdd** and **vio** is not maintained, Intel strongly recommends a series resistor in **vio** be used to limit any excess current.

a. not required on 21555

1.3.2 Miscellaneous Features

Selectable bus parking at either the 21555 or last master leads to improvements in bus performance when one device on the bus generates more traffic than others.

Table 3. New JTAG Signal Requirement

tms	I	The JTAG test mode select pin, **tms** causes state transitions in the Test Access Port (TAP) controller. The **tms** signal is pulled high by a weak pull-up resistor internal to the device. If this pin is low while **t_rst_l** is low the device can enter an unsupported mode. Other devices that are not on early power and are connected to the JTAG Scan Chain, pull **tms** low during Hot Insertion causing the 21555 to enter the unsupported mode. During the Hot Insertion isolate this signal from other JTAG devices on the circuit board or JTAG scan chain.

Table 4. Secondary Bus Feature

s_rst_in_l	in	This is an alternate reset input for the 21555. This causes the same action as if **p_rst_l** were asserted. These signals are ORed on chip. All configuration modes are captured on this edge. Allows for a reset initiated from the secondary bus, or a board reset for hot swap. Results in **s_rst_l** being asserted, but the **p_rst_l** pin is not affected.

Table 5. Bus Arbiter and Clock Output Features

s_clk_o	out	New Feature: Buffered version of **p_clk**. the 21555 divides **p_clk** by two (2) to generate **s_clk_o** when **p_m66ena** is sampled high and **s_m66ena** is sampled low (primary operating at 66MHz and secondary operating at 33MHz).
p_clk **s_clk**	in	New Feature: These are the primary and secondary interface clock signals. They provide timing for all transactions on the respective PCI bus. All PCI inputs are sampled on the rising edges of the **p_clk** or **s_clk** signals and are supported by the 21555 at frequencies up to 66MHz.
p_m66ena	in	When asserted, indicates that the primary interface is operating at 66MHz.
s_m66ena	in/od	New Feature: When asserted, indicates that the secondary interface is operating at 66MHz. The 21555 pulls down this signal when the primary interface is operating at 33MHz (**p_m66ena** low) and the secondary clock output **s_clk_o** is enabled.

Table 6. ROM Interface Signal Features

pr_ad[1]	The value of **pr_ad[1]** signals during chip reset specify the configuration options listed below. The values of configuration options **pr_ad [7:1]** may be read from the Mode Settings configuration register. See Table 15 on page 14. New Feature: **pr_ad[1]:** If the **s_rst_in_l** signal is used to reset the chip, sampling this signal low upon deassertion of **s_rst_in_l** enables the primary bus 64-bit extension. Sampling this signal high upon deassertion of **s_rst_in_l** disables the primary bus 64-bit extension, and those signals are then driven to valid logic values.

Table 7. Hot-Swap Signal Features

l_stat	TS	This is the Compact PCI hot-swap local status pin. This 21555 input signal indicates the sense of the ejector switch and therefor the state of the LED on the Compact PCI card that supports distributed hot-swap. Two (2) ms of de-bounce is implemented on this pin. As a 21555 output it controls the LED. When the add in card does not support Compact PCI hot-swap, pull this signal low through a resistor.

1.4 Read and Write Transactions

This section describes the following transactions:

- Section 1.4.1, “Posted Write Transactions”.
- Section 1.4.2, “Delayed Write Transactions”.
- Section 1.4.3, “Delayed Read Transactions”.

1.4.1 Posted Write Transactions

If the 21555 receives 2^{24} consecutive target retries from the target when attempting to deliver posted write data, then the 21555 discards the posted write transaction and conditionally asserts **SERR#** on the initiator bus.

New Feature

This retry counter may be disabled by setting the Retry Counter Disable bit in the Chip Control 0 configuration register. The 21555 also conditionally asserts **SERR#** on the initiator bus if a target abort or master abort is detected on the target bus in response to the posted write.

1.4.2 Delayed Write Transactions

The 21555 requests the target bus and initiates the delayed write transaction as soon as the 21555 ordering rules allow. The 21555 always performs a single 32-bit data phase when initiating a delayed write transaction. The 21555 completes the transaction on the target bus and adds the completion status to the queue. Completion status contains the type of termination (**TRDY#**, target abort, master abort) and whether **PERR#** assertion was detected.

This phase of the delayed transaction is called the delayed write completion (DWC). If the 21555 receives 2^{24} consecutive target retries from the target, then the 21555 discards the delayed write request and conditionally asserts SERR# on the initiator bus.

New Feature

This retry counter may be disabled by setting the Retry Counter Disable bit in the Chip Control 0 configuration register.

If the transaction is discarded before completion, the 21555 returns a target abort to the initiator.

1.4.3 Delayed Read Transactions

If the 21555 receives 2^{24} consecutive target retries from the target, the 21555 discards the delayed read transaction and conditionally asserts SERR# on the initiator.

New Feature

This retry counter may be disabled by setting the Retry Counter Disable bit in the Chip Control 0 configuration register. If the transaction is discarded before completion, the 21555 returns a target abort to the initiator.

1.5 Lookup Table Based Address Translation

The Upstream Memory 2 address range consists of a fixed number (64) of pages. The page size is programmable in the Chip Control 1 configuration register. Therefore, the size of the Upstream Memory 2 BAR is dependent on the page size.

New Feature

The page size varies between 256-bytes to 32-Mbytes by powers of two (2). This results in a window size that varies from 16-Kbytes to two (2)-Gbytes. This BAR can also be disabled. This improvement allows upstream access of the full four(4)-Gbyte system memory using all of the upstream bars.

1.6 Initiation of Configuration Transactions by the 21555

If the Delayed Transaction Target Retry Counter expires, that is, 2^{24} target retries are received from the target, then the 21555 returns a target abort to the initiator.

New Feature

The Delayed Transaction Target Retry Counter may be disabled, and thus does not limit the number of retries, by setting the Retry Counter Disable bit in the Chip Control 0 configuration register.

New Feature

The 21555 can be enabled to respond to configuration transactions that it generates by setting the appropriate Downstream or Upstream Self-Response Enable bit in the Configuration Control and Status register. In order for the 21555 to respond, the transaction must assert the 21555's IDSEL signal on that interface, and it is a Type 0 configuration transaction. If this bit is not set, the 21555 will not respond to any configuration transactions that it generates, and these transactions may end in master abort.

2.0 New Register Features

The new features and differences of the 21555 registers are discussed in the following tables:

- Table 8, "Vendor ID Register".
- Table 9, "Device ID Register".
- Table 10, "Bit 31 of the Base Address Register (BAR)".
- Table 11, "Configuration Control and Status".
- Table 12, "Chip Control - 0 Register".
- Table 14, "Arbiter Control Register".

Table 8. Vendor ID Register

• Primary byte offset: 01:00h and 41:40h. • Secondary byte offset: 41:40h and 01:00h.			
Bit	**Name**	**R/W**	**Description**
15:0	Vendor ID	R	The Vendor ID identifies Intel® as the vendor of this device and is internally hardwired to be 8086 hex.

Table 9. Device ID Register

- Primary byte offset: 03:02h and 43:42h.
- Secondary byte offset: 43:42h and 03:02h.

Bit	Name	R/W	Description
15:0	Device ID	R	Device ID identifies this device as the 21555 and is internally hardwired to be B555h.

Table 10. Bit 31 of the Base Address Register (BAR)

	Downstream			Upstream
Byte Offset	**Memory 0**	**Memory 2**	**Memory 3**	**Memory 1**
Primary	AF:ACh	B7:B4h	BB:B8h	CB:C8h
Secondary	AF:ACh	B7:B4h	BB:B8h	CB:C8h

Bit	Name	R/W	Description
31	**BAR_Enable**	R/(WS)	Base Address Register enable. • *When 0:* The corresponding BAR is disabled and reads as 0, with the two following exceptions. • *When 1:* The corresponding BAR is enabled, with size and type specified by this setup register. *Reset value:* 0, except for Downstream Memory 0 Setup register, whose value is always 1.
New Feature: Exceptions			Bit [31] of the Downstream Memory 0 Setup register always reads one (1), indicating that the BAR cannot be disabled. • If a bus master attempts to write this bit with a 0, the 21555 will return all bits [31:12] of the setup register as 1s (request 4K). • If the upper 32 Bits of the Downstream Memory 3 Setup register bit [31] is a 1, then the corresponding BAR is enabled as a 64-bit register, and this bit is part of the size field for the 64-bit BAR.

Table 11. Configuration Control and Status

- Primary Byte offset: 93:92h.
- Secondary Byte offset: 93:92h.
- CSR Byte Offset: 013:012h.

Bit	Name	R/W	Description
2	Downstream Self-Response Enable	R/W	New Feature: Controls the 21555's ability to respond to a configuration transaction that it generates as a master. • *When 0:* The 21555 does not respond to configuration transactions that it generates. These transactions end in master abort. • *When 1:* The 21555 does respond to configuration transactions that it generates as a master. *Reset value:* 0
10	Upstream Self-Response Enable	R/W	New Feature: Controls the 21555's ability to respond to a configuration transaction that it generates as a master. • *When 0:* The 21555 does not respond to configuration transactions that it generates. These transactions end in master abort. • *When 1:* The 21555 does respond to configuration transactions that it generates as a master. *Reset value:* 0

Note: This register may be preloaded by serial ROM or programmed by the local processor before host configuration.

Table 12. Chip Control - 0 Register

- Primary byte offset: CD:CCh.
- Secondary byte offset: CD:CCh.

Bit	Name	R/W	Description
12	LUT Page Size Extension Bit	R/W	New Feature: Allows selection of larger page sizes when programming the Page Size field in the Chip Control 1 configuration register. • *When 0:* Page sizes 256-bytes through four (4)-Mbytes are available in the Page Size field. New Feature: • *When 1:* Page sizes eight (8)-Mbytes through 32-Mbytes are available in the Page Size field. Reset value is zero (0)

Table 13. Bits 11:8 of the Chip Control 1 Register and Bit 12 of Chip Control 0 Register

• Primary byte offset: CF:CEh. • Secondary byte offset: CF:CEh.			
11:8	Page Size	R/W	This field selects the page size used for the Upstream Memory 2 address range. The total size of this range is dependent on the page size. Page size values and their encoding depend on the value of the LUT Page Size Extension bit [12] which is described in Table 12. Reset value is zero (0)

If Bit 12 is Zero (0)		**If Bit 12 is One (1)**	
11:8 Value	**Page Size**	**11:8 Value**	**Page Size**
0h	Disables Upstream memory 2 Base Address Register	0h	Disables Upstream memory 2 Base Address Register
1h	256-bytes	1h	Eight (8)-Mbytes
2h	512-bytes	2h	16-Mbytes
3h	1-Kbyte	3h	32-Mbytes
4h	2-Kbyte	4h through Fh will disable the upstream base address register	
5h	4-Kbyte		
6h	8-Kbyte		
7h	16-Kbyte		
9h	32-Kbyte		
10h	64-Kbyte		
Ah	128-Kbyte		
Bh	256-Kbyte		
Ch	512-Kbyte		
Dh	One (1)-Mbytes		
Eh	Two(2)-Mbytes		
Fh	Four(4)-Mbytes		

Table 14. Arbiter Control Register

• Primary byte offset: D3:D2h. • Secondary byte offset: D3:D2h.			
Bit	**Name**	**R/W**	**Description**
10	Bus Parking Control	R/W	New Feature: Controls whether the 21555 parks on itself or on the last master to use the bus. • *When 0:* During bus idle, the 21555 parks the bus on the last master to use the bus. • *When 1:* During bus idle, the 21555 parks the bus on itself. The bus grant is removed from the last master and internally asserted to the 21555. *Reset value:* 0b

Table 15. Mode Setting Configuration Register

This register reflects the various mode settings selected by strapping the **pr_ad** pins, as well as whether the 64-bit extension is enabled.

- Primary byte offset: D6h.
- Secondary byte offset: D6h.

Bit	Name	R/W	Description
0	Serial Preload Enabled	R	Indicates whether a serial preload was performed. *When 0*: The serial preload enable sequence was not detected and the register preload was not performed. *When 1*: The serial preload enable sequence was detected and the register preload was performed.
1	Primary Lockout Reset Value	R	Indicates the primary lockout reset value determined by sampling **pr_ad[3]** during reset. *When 0:* Signal **pr_ad[3]** was sampled low, causing the Primary Lockout bit to be low upon completion of chip reset. *When 1:* Signal **pr_ad[3]** was sampled high, causing the Primary Lockout bit to be set high upon completion of chip reset.
2	Synchronous Enable	R	Indicates whether synchronous or asynchronous mode was selected by sampling **pr_ad[4]** during reset. *When 0*: Signal **pr_ad[4]** was sampled low, selecting synchronous mode. *When 1*: Signal **pr_ad[4]** was sampled high, selecting asynchronous mode.
3	**s_clk_o** Enable	R	Indicates whether **s_clk_o** is enabled, determined by sampling **pr_ad[5]** during reset. *When 0:* Signal **pr_ad[5]** was sampled low, causing **s_clk_o** to be disabled. *When 1:* Signal **pr_ad[5]** was sampled high, causing **s_clk_o** to be enabled.
4	Secondary Central Function Enable	R	Indicates whether secondary bus central functions are enabled, determined by sampling **pr_ad[6]** during reset. *When 0:* Signal **pr_ad[6]** was sampled low, causing secondary central functions to be enabled. *When 1:* Signal **pr_ad[6]** was sampled high, causing secondary central functions to be disabled.
5	Arbiter Enable	R	Indicates whether the secondary bus arbiter is enabled, determined by sampling **pr_ad[7]** during reset. *When 0:* Signal **pr_ad[7]** was sampled low, causing the secondary bus arbiter to be disabled. *When 1:* Signal **pr_ad[7]** was sampled high, causing the secondary bus arbiter to be enabled.
6	Primary 64-Bit Extension	R	Indicates whether the primary bus 64-bit extension is enabled. *When 0:* The primary bus 64-bit extension is disabled. *When 1:* The primary bus 64-bit extension is enabled.
7	Secondary 64-Bit Extension	R	Indicates whether the secondary bus 64-bit extension is enabled. *When 0:* The secondary bus 64-bit extension is disabled. *When 1:* The secondary bus 64-bit extension is enabled.

Table 16. CLS Information (Bits 1 and 2 of the Chip Control 1 Register)

0	Primary Posted Write Threshold	R/W	Controls the queue full threshold limit of the downstream posted write queue. When the queue is designated full, the 21555 returns retry to posted writes on the primary bus. Otherwise, the 21555 accepts write data into the posted write queue. • When 0, Posted write queue full when less than a cache line is free to post data. • When 1, Posted write queue full when less than a half cache line (for CLS=8,16,32) is free to post data. • Reset value – 0b
1	Secondary Posted Write Threshold	R/W	Controls the queue full threshold limit of the upstream posted write queue. When the queue is designated full, the 21555 returns retry to posted writes on the secondary bus. Otherwise, the 21555 accepts write data into the posted write queue. • When 0, Posted write queue full when less than a cache line is free to post data. • When 1, Posted write queue full when less than a half cache line (for CLS=8,16,32) is free to post data. • Reset value – 0b

Table 17. Primary and Secondary Cache Line Size Registers

Offsets	Primary Cache Line Size	Secondary Cache Line Size
Primary byte	0Ch	4Ch

Bit	Name	R/W	Description
7:0	Cache Line Size	R/W	Designates the cache line size for the corresponding interface in units of 32-bit Dwords. Used for prefetching memory reads and for terminating MWIs. Valid cache line sizes are 8, 16, and 32 Dwords. When the cache line size is set to any other value, the 21555 uses the same behavior as when the cache line size is set to 8. Reset value – 00h.

3.0 I2O and Indirect Transaction Support

This section describes the following features:

- Section 3.1, “Generic Own Bits”.
- Section 3.2, “Internal Arbitration”.
- Section 3.3, “66MHz Support”.
- Section 3.4, “Central Function During Reset”.
- Section 3.5, “CompactPCI Hot Swap State Machine”.

3.1 Generic Own Bits

New Feature

The 21555 implements two generic Own Bits that can be accessed in either memory or I/O space from either the primary or secondary interface. These bits are an aid to lock resources in software. The Own Bit will automatically set the bit upon completion of the read. When a bus master reads the Own Bit, it will return:

- A one (1) if it has already been set.
- A zero (0) if the Own Bit is available.

The Own Bit is cleared by writing a one (1) to the bit. In order to check the status of an Own Bit without causing the bit to set, a read-only shadow copy of the bit can be read

- Own Bit 0 is bit [0] at CSR offset 0D0h, bits [7:1] are reserved.
- Own Bit 1 is bit [0] at CSR offset 0d1h, bits [7:1] are reserved.

Shadow copies of these Own Bits may be found at bits [1:0] at CSR offset 0D2h. In order to prevent unintended side effects, byte access of these fields should be used.

This feature is especially useful in doing indirect configuration or I/O access across two 21555 devices that are cascaded or connected in a primary to secondary configuration. It allows atomic access to device configuration registers by two processors in the special case where two 21555 devices are involved. Support for this would be implemented in memory for the 21554.

The 21554 and the 21555 have Configuration Own Bit semaphores. These are for atomic access of device configuration space for two processors when only one 2155X is in the design.

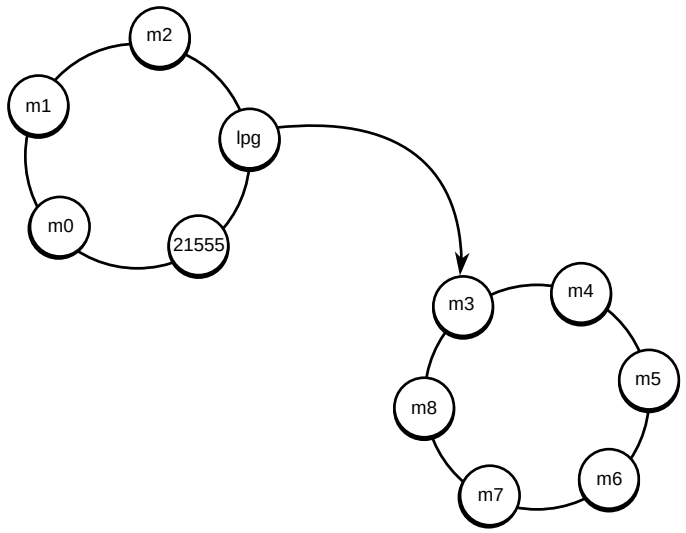
3.2 Internal Arbitration

Figure 2 the 21555 secondary arbitration flow. Each bus master, including the 21555, may be configured to be in either the low priority group or the high priority group by setting the corresponding priority bit in the Arbiter Control register in device specific configuration space. If that bit is a:

- One (1), the master is assigned to the high priority group.
- Zero (0), the master is assigned to the low priority group.

If all masters are assigned to one group, then the algorithm defaults to a straight rotating priority among all the masters. After reset, all external masters are assigned to the low priority group and the 21555 is assigned to the high priority group. The 21555 receives highest priority on the target bus every other transaction and priority rotates evenly among the other masters.

Figure 2. 21555 Secondary Arbiter



m#	=	Master number
lpg	=	Low priority Group
Arbiter Control Register	=	100000111

Priorities are reevaluated every time **s_frame_l** is asserted, for example at the start of each new transaction on the secondary PCI bus. From this point until the time that the next transaction starts, the arbiter asserts the grant signal that corresponds to the highest priority request that is asserted. If a grant for a particular request is asserted and a higher priority request subsequently asserts; the arbiter will deasserts the asserted grant signal and assert the grant corresponding to the new higher priority request on the next PCI clock cycle.

New Feature

The 21555 does guarantee a two-cycle minimum assertion time during bus idle once a grant is asserted to a bus master. When priorities are reevaluated, the highest priority is assigned to the next highest priority master relative to the master that initiated the previous transaction. The master that initiated the last transaction has the lowest priority in its group.

The arbiter deasserts the grant if the 21555 detects that a master has failed to assert **s_frame_l** after sixteen cycles of both grant assertion and a secondary idle bus condition. That master does not receive any more grants until it deasserts its request for at least one PCI clock cycle.

In order to prevent bus contention, if secondary **FRAME#** is deasserted, the arbiter never asserts one grant signal in the same PCI cycle as it deasserts another. It deasserts one grant, and then assert the next grant no earlier than one PCI clock cycle later. If **s_frame_l** is asserted, then the arbiter may deassert one grant and assert another grant during the same PCI clock cycle.

New Feature

The 21555's internal arbiter may be programmed to park the secondary PCI bus either at the last master to use the bus, or always on the 21555. In the former case, an initiator's secondary bus grant remains asserted unless and until another initiator has asserted its secondary bus request. In the latter case, if no requests are asserted once a transaction has begun the bus grant is withdrawn from the last master and is asserted internally to the 21555. After reset, the internal arbiter always parks the secondary bus at the 21555.

For secondary bus Internal Arbitration, the 21555 arbitration signal pairs [5:8] are disabled for 66MHz operation.

3.3 66MHz Support

New Feature

The 66MHz capable 21555 has two pins, **p_m66ena** and **s_m66ena**, which indicate whether the primary and secondary bus are operating at 66MHz, respectively.

- **p_m66ena** is an input only pin.
  - — When high, the primary bus is assumed to be operating at 66MHz.
  - — When low, the primary bus is operating at or below 33MHz.
- **s_m66ena** is an input-open-drain pin.
  - — When high, the secondary bus is assumed to be operating at 66MHz.
  - — When low, the secondary bus is operating at or below 33MHz.

The 21555 pulls **s_m66ena** low when the primary bus is operating at 33MHz, **p_m66ena** is low, and **s_clk_o** is enabled. When **s_clk_o** is enabled it is assumed that the 21554 is controlling the clocking of the secondary bus, and since **s_clk_o** is a buffered version of **p_clk** it must operate at 33MHz.

When **p_m66ena** is sampled high, **s_m66ena** is sampled low, and **s_clk_o** is enabled, the 21555 divides **s_clk_o** by two (2) to generate a 33MHz clock.

The 21555 can handle any combinations of clock frequencies between the primary and secondary buses with the maximum clock ratio between the primary and secondary buses being 2.5:1. For example: 25MHz on one bus and 66MHz on the other, and a maximum frequency of 66MHz.

3.4 Central Function During Reset

The 21555 is selected as the secondary bus central function when it detects a low **pr_ad[6]** and an asserted **s_rst_l**. This condition, immediately drives **s_ad**, **s_cbe_l**, and **s_par** low and tri-states the secondary bus control signals for the duration of secondary bus reset. If the 21555 implements a 64-bit secondary interface, it also asserts **s_req64_l**, but tri-states all secondary bus 64-bit extension signals. The 21555 is always a secondary bus 64 bit master when it is the central function agent.

If **pr_ad[6]** is detected high during **s_rst_l** assertion, then another device is acting as a central function on the secondary bus. The 21555 tri-states all secondary PCI signals, including **s_ad**, **s_cbe_l**, and **s_par,** for the duration of secondary bus reset. The 21555 does not assert **s_req64_l**

during reset, therefore an external agent must assert **s_req64_l** to enable the 21554's secondary interface 64-bit extension. If the central function agent does not assert **s_req64_l** on the rising edge of **s_rst_l** then the 21554's secondary interface is 32 bit mode.

New Feature

The assertion of **s_rst_in_l** asynchronously asserts **s_rst_l**. If enabled the secondary bus central functions continue to activate upon assertion of **s_rst_l**. The primary PCI 64 bit extension signals are disabled by strapping **pr_ad[1]** high on the rising edge of **s_rst_in_l**.

3.5 CompactPCI Hot Swap State Machine

Figure 3 shows the flow of the CompactPCI hot swap machine state. When **l_stat** goes high and the **INS_STAT** bit is cleared, it indicates that the ejector handle has been opened. This is interpreted as a removal event, and the 21555 enters the signal removal state. The same happens when the 21555 samples **I_STAT** high while in the normal operation state.

Figure 3. Hot Swap Insertion and Removal Flowchart